

REMARKS/ARGUMENTS

Claims 1-5, 7-15 and 17-29 are pending in the application. Claims 1-5, 7-15 and 17-27 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,763,363 to Driscoll. New claims 28 and 29 are herewith presented for examination.

Driscoll fails to anticipate claims 1-5, 7-15 and 17-29 under 35 U.S.C. 102(e), as it fails to disclose each element of the claimed invention. Consider claim 28, which includes the system of claim 1 wherein the memory controller that directs digital data from the memory to the data buffer with the digital data passing through the encryption key generator prior to entering the input/output register comprises means for encrypting the digital data prior to entering the input/output register. This claim invokes the provisions of 35 U.S.C. 112(6), and thus incorporates the structure disclosed in the specification for performing the corresponding function. Driscoll fails to disclose this structure or an equivalent thereof. Applicant respectfully submits that claim 28 is allowable over Driscoll.

Likewise, claims 2 and 13 as amended and new claim 29 include “an inaccurate clock,” which as described in the specification provides non-obvious advantages over the prior art such as Driscoll, which both utilizes and requires an accurate clock. Applicant respectfully submits that claims 2, 13 and 29 are allowable over Driscoll.

Claim 1 includes a memory controller that directs digital data from the memory to the data buffer with the digital data passing through the encryption key generator prior to entering the input/output register. The Examiner cites to col. 4, lines 30-40 of Driscoll as disclosing this limitation, which is reproduced here in its entirety: “One form of a stream cipher cryptosystem according to the present invention includes a PRNG receiving a key and providing a keystream. The PRNG includes a word-by-word shifting LFSR according to the present invention for providing a LFSR output word of word length M. The stream cipher cryptosystem also includes a cryptographic combiner for combining a first binary data sequence and the keystream to provide a second binary data sequence. In encryption operations, the cryptographic combiner is an encryption combiner and the first binary data sequence is a plaintext binary data sequence and the second binary data sequence is a ciphertext binary data sequence.” As disclosed at col. 3, line 41 of Driscoll, the LFSR is “implemented in software,” which means that it is operating on a processing unit such as the computer system of sender 22 of Driscoll. Claim 1, as amended, includes an integrated encryption key generator. As such, the PRNG of Driscoll, which includes

a word-by-word shifting LFSR that is implemented in software operating on a processing unit, can not disclose a memory controller that directs digital data from the memory to the data buffer with the digital data passing through the integrated encryption key generator prior to entering the input/output register. Applicant respectfully submits that claim 1, as amended, is allowable over Driscoll.

In regards to claims 3-5 and 7-8, Applicant believes that the limitations of these claims reinforce what has been made explicit in amended claim 1, namely, that these claims pertain to systems implemented in hardware that are not anticipated by the software implemented system of Driscoll, and are allowable for that reason, as well as for the reason that they depend from an allowable base claim and add limitations not found in the prior art. Applicant respectfully submits that claims 3-5 and 7-8 are allowable over Driscoll.

Claim 9 includes an encryption circuit with a plurality of keys that decrypts the encrypted digital data in response to the memory request of the memory controller. As previously discussed, Driscoll discloses a system that is implemented in software, and does not disclose any circuitry whatsoever, much less an encryption circuit with a plurality of keys that decrypts the encrypted digital data in response to the memory request of the memory controller. It is noted that the materials relied on by the Examiner at col. 5, lines 33-55 of Driscoll as allegedly disclosing the limitations of claim 9, explicitly require the operation of PRNG 44 of Driscoll, which, as discussed, explicitly requires the operation of the word-by-word shifting LFSR that is implemented in software operating on a processing unit. Applicant respectfully submits that claim 9 is allowable over Driscoll.

Claim 12 includes a method of digital data encryption in a digital device, comprising generating at least one key; placing the digital data in a data buffer; and encrypting the digital data using the at least one key while the digital data is being placed in a rewritable memory. Again, the materials relied on by the Examiner unmistakably reinforce that the system of Driscoll is a software implemented system operating on a processing unit, which means that Driscoll simply cannot disclose placing the digital data in a data buffer and encrypting the digital data using the at least one key while the digital data is being placed in a rewritable memory. The use of different terms “data buffer” and “rewritable memory” creates a presumption that these terms connote different meanings. *CAE Screenplates Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000) (“In the absence of any evidence to the contrary, we must

presume that the use of these different terms in the claims connotes different meanings."); *Applied Med. Res. Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324, 1333 n.3 (Fed. Cir. 2006) ("[T]he use of two terms in a claim requires that they connote different meanings. . . ."). As such, whether the memory of the processing unit of Driscoll is characterized as a "data buffer" or a "rewritable memory," it cannot be both, such that Driscoll fails to disclose each element of claim 12. Applicant respectfully submits that claim 12 is allowable over Driscoll.

Claim 22 as amended includes a method to decrypt encrypted digital data stored in memory of a digital device, comprising: generating a memory request to retrieve the encrypted digital data; and decrypting the encrypted digital data using at least one key. Again, the materials relied on by the Examiner as anticipating claim 22 are in fact a description of the software implemented processes previously discussed, which, taking place on and within a processing unit, simply cannot relate to data stored in memory of a digital device, as data is not stored in encrypted form in a processing unit. Applicant respectfully submits that claim 22 is allowable over Driscoll.

Claim 25 includes an encryption circuit with at least one key. Again, the materials relied on by the Examiner confirm that Driscoll discloses an encryption process that is implemented in software and thus operates on a processing unit, and does not disclose any circuitry, much less an encryption circuit with at least one key. Applicant respectfully submits that claim 25 is allowable over Driscoll.

Any claims not explicitly addressed are believed to be allowable at least for the reasons discussed above as well as because they depend from an allowable base claim and add limitations not present in the prior art.

**CONCLUSION**

In view of the foregoing remarks and for various other reasons readily apparent, Applicant submits that all of the claims now present are allowable, and withdrawal of the rejection and a Notice of Allowance are courteously solicited.

If any impediment to the allowance of the claims remains after consideration of this amendment, a telephone interview with the Examiner is hereby requested by the undersigned at (214) 953-5990 so that such issues may be resolved as expeditiously as possible.

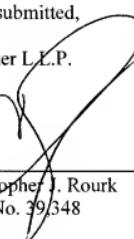
A Petition for 1-Month Extension of Time is filed herewith. Please charge the extension fee in the amount of \$120.00 to Deposit Account No. 50-0835. The Commissioner is hereby authorized to charge any fee or credit any refund to Deposit Account No. 50-0835.

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Respectfully submitted,

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